WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a first signal path that transfers a first signal supplied from outside;

a second signal path that transfers a second signal supplied from outside; and

at least one pulse generator that forms a first pulse corresponding to a difference in phase between the first signal and the second signal in response to the first signal and the second signal,

wherein the number of buffer stages provided in the first signal path and the second signal path is greater than the number of combination circuit stages provided in the pulse generator.

2. A semiconductor integrated circuit device comprising:

a first signal path that transfers a first signal supplied from outside;

a second signal path that transfers a second signal supplied from outside; and

at least one pulse generator that forms a first pulse corresponding to a difference in phase between the first signal and the second signal in response to the first signal and the second signal,

wherein a whole wiring length of the first signal path

and the second signal path is longer than a wiring length between the pulse generator and a circuit to which the pulse is transferred.

3. A semiconductor integrated circuit device comprising:

a first signal path that transfers a first signal supplied from outside;

a second signal path that transfers a second signal supplied from outside; and

at least one pulse generator that forms a first pulse corresponding to a difference in phase between the first signal and the second signal in response to the first signal and the second signal,

wherein a rising time up to full amplitude at any one of buffers in the first signal path and the second signal path is longer than a pulse width of the first pulse.

4. A semiconductor integrated circuit device according to claim 3, further comprising a third signal path supplied with a third signal from an external terminal,

wherein the pulse generator forms a second pulse corresponding to a difference in phase between the second signal and the third signal.

5. A semiconductor integrated circuit device according to claim 4, further comprising combination circuits and LSSD type flip-flops respectively provided on

the input and output sides of the combination circuits,

wherein the first pulse and the second pulse are used in an AC test operation of said each combination circuit.

6. A semiconductor integrated circuit device according to claim 5, wherein the first signal path, the second signal path and the third signal path extend in a direction parallel to each other and are placed adjacent to each other, and includes the same number of buffer stages, and

the pulse generator outputs clock the first pulse and second pulse for an AC test for said each combination circuit, and clock pulses for serially transferring a test input signal and a test output signal to said each LSSD type flip-flop in a test mode, and

outputs any one of the first through third signals as a clock pulse upon a normal operation.

7. A semiconductor integrated circuit device according to claim 6, wherein a clock pulse at the normal operation is transferred through a signal path interposed between the two of the first signal path through the third signal path extended in parallel adjacent to one another, and signal paths disposed on both sides are respectively set to a fixed potential.

8. A semiconductor integrated circuit device according to claim 3, wherein each of elements that

constitute the buffers provided in the first and second signal paths and the pulse generator comprises a MOSFET having a metal gate structure.